

POLYIMIDE BASED AMORPHOUS SILICON SOLAR MODULES <sup>1</sup>

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Requirements for space power are increasingly emphasizing lower costs and higher specific powers. This results from new fiscal constraints, higher power requirements for larger applications and the evolution toward longer distance missions such as a Lunar or Mars base. The polyimide based a-Si modules described in this paper are being developed to meet these needs. The modules consist of tandem a-Si solar cell material deposited directly on a roll of polyimide. A laser scribing/printing process subdivides the deposition into discrete cell strips which are series connected to produce the required voltage without cutting the polymer backing. The result is a large, monolithic, blanket type module approximately 30 cm wide and variable in length depending on demand. Current production modules have a specific power slightly over 500 W/Kg with room for significant improvement. Costs for the full blanket modules range from \$30/Watt to \$150/Watt depending on quantity and engineering requirements. Work to date has focussed on the modules themselves and adjusting them for the AM0 spectrum. Work is needed yet to insure that the modules are suitable for the space environment.

## Introduction

This project, initiated in 1990, is designed to simultaneously develop a lightweight flexible PV technology suitable for space application and the process for producing large arrays from that technology. The product is a monolithically integrated amorphous silicon module, fabricated directly on a polyimide blanket.

Benefits of this technology include extremely high power to weight ratios and low potential costs. The high specific power results from the ability to deposit the thin film cells directly on a polyimide substrate. The low potential costs are due to the low material costs of the thin film approach and the economic benefits of full roll-to-roll processing. Attainment of low costs is predicated on high volume production (>1MW/yr) which will require piggybacking manufacturing of space cells on manufacturing for terrestrial applications.

Another group of benefits relate to the basic nature of the product. The material comes already integrated into large area modules. This greatly simplifies full system assembly and thus reduces full system costs. The flexible nature of the material provides a wide range of stowage and deployment options which may translate into improved costs and reliability. The combination of amorphous material and polymer substrate make a robust module which will not be easily damaged by launch shocks or impacts. This feature improves reliability and can reduce launch weight by eliminating some of the protective measures required for more fragile type cells.

<sup>1</sup> This work is partially sponsored by NASA Lewis Research Center under contract # NAS3-26244

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The principal price paid for these benefits is conversion efficiency. While the weight and cost per watt are significantly lower than for other technologies, the area required for an application will be increased. This shortcoming will limit the applications of the product. Use in lower orbits, where drag is significant, will probably have to be limited to back-up power or to short duration flights.

The benefits of this material will become more significant as mission distance increases and power demands increase. In these cases, weight and cost will become the stronger driving factors.

### Device Structure

Currently, the tandem a-Si device structure shown in figure 1 is being deposited on 2 mil thick polyimide substrate. Both i layers in this structure are a-Si:H material while all doped layers are microcrystalline.

The key features in maximizing performance of this structure, outside of basic material quality are: 1) maximizing transmission through the TCO and P+ top layers. 2) Insuring the adequacy of doped layers to provide full voltage. 3) Providing high recombination rates in the tunnel junction to minimize resistance and voltage loss. 4) Maximizing reflectance and scattering of red light off the back metal contact. 5) Balancing the thicknesses of the two i layers to insure current matching under the AM 0 spectrum.

Minimizing absorption in the top p+ layer and insuring adequate thickness and doping to achieve full voltage are competing elements. Thicker and more heavily boron doped layers absorb more of the incoming blue and near UV light. We have chosen a microcrystalline p+ layer to minimize this absorption. Achieving a good microcrystalline layer is very sensitive to many system design and deposition parameters. Figure 2 demonstrates this, showing Quantum Efficiency (Q.E.) curves for two single junction samples with slightly different p+ deposition conditions. A significant difference is seen in the blue response of these devices which correlates with a 10 % difference in device current. Neither curve shows a very good blue response. Calculations indicate that further work in this areas could yield another 20% improvement in current.

The tunnel junction must provide for recombination of the electrons injected from the top device and holes coming from the bottom device. The recombination rate must be fast enough that no reverse voltage is generated at the p+ n+ interface. To achieve this, highly degenerate layers are required and must have adequate thickness. Figure 3a shows an I-V curve for a single junction device with an n+ layer on top to form a tunnel junction. The double-back curve is a signature of a reverse junction at the p+ n+ interface indicating inadequate doping or thickness of one of the layers. It was determined in this case that the p+ layer was inadequate. Figure 3b shows the I-V curve of a later cell with adequate doping.

Optimum utilization of the red end of the spectrum can be achieved by maximizing reflection and scattering off the back metal contact. Scattering provides the longest path length within the semiconductor material while high reflectance reduces the energy lost to absorption in the back metal. Figure 4 shows Q.E. curves for a device on specular metal and on our current textured back metal contact. This figure also shows a Q.E. curve for optimized light trapping for a superstrate cell with silver/SnO<sub>2</sub> back contact from Solarex. (1) Current texturing is clearly having an effect, however there is still improvement to be made. Calculations show another 20 % improvement in current over our current devices appears achievable.

Balancing the thicknesses of the i layers to match currents under an AM 0 spectrum is required for maximum cell output. This process must be redone after any of the cell improvement modifications discussed above. Table 1 demonstrates the dependence of optimum layer thicknesses on spectral distribution. The table gives the short circuit currents under ELH and LAPPS illumination for three tandem samples with different thickness top i layers. The ELH spectrum is heavy in the red end while the LAPSS spectrum is heavier in the blue and UV, more closely simulating AM0. The optimum thickness for the ELH spectrum appears to be in the range of 850 Å to 900 Å, while the optimum for the LAPSS spectrum is closer to 670 Å. From this data, the optimum for LAPPS may even be significantly less than 670 Å. Improvement in the blue response of the device will call for reducing the top i layer thickness, while improvement in the red response will call for a thicker layer.

## Module Structure

To achieve the large area modules, cells are subdivided without cutting the polyimide substrate and interconnected as shown in figure 5. The first laser scribing step defines individual cells by cutting the combined back metal contact and a-Si device layers. Two insulating ink lines are then printed to protect against shorting in the first scribe cut and to act as a beam stop for next laser scribe. The TCO is next deposited over the a-Si device layer and the ink lines. Next, conductive ink grid lines are printed over the TCO. To finish the interconnect system, the laser is used to cut the TCO over the second ink line and to weld between the top and bottom layers in the interconnect area.

Currently, maximum substrate width is 13" and maximum web length is 500 ft. This could be configured into a single module 13" wide by 500 ft long, but would, in most cases, be cut into smaller strips. Our typical interconnect results in a module voltage of 10 Volts per linear ft so that a 1 ft wide by 10 ft long module would operate at 0.5 Amps and 100 Volts. Interconnects can easily be varied by changing the print patterns and the laser scribing program. This allows modules with a wide range of currents and voltages to be produced.

As a result of the fabrication process, the basic unit of this technology is not a single cell, but a large area module blanket. It is important to recognize that all cell parameters are applicable to full blankets or wings (minus support structures) and should be compared to full blanket arrays of competing technologies rather than to individual cell parameters. This applies to \$/Watt, Watts/ Kg and Watts/ M<sup>2</sup>.

## Performance

Figure 6 show and I-V curve for the current level of device coming off the manufacturing line. Table 2 shows performance parameters for the full modules. The first column give the current parameters. The second column give the parameters expected within the next few years. The third column gives an estimate of the potential of the technology.

## Future Work

There is considerable work yet to be done to make this product ready for space use. This includes device processing development and space qualification work.

Significant efficiency improvement is possible by improving materials and processing. Short circuit current can be improved by improving the p+ layer transmission, the back metal contact reflectance, deposition of an index matching layer on top of the TCO, and reducing the interconnect areas though tighter alignment. Open circuit voltage and fill factor can be increased by improving the p+/i interfaces and the tunnel junction.

Space qualification tests are yet to be started. Of particular need are thermal shock tests, radiation resistance and light induced degradation under space conditions.

## Conclusions

The capability has been developed for fabricating large area arrays of tandem a-Si devices on polyimide substrates. Performance of material currently being manufactured provides very high specific power ratios and low cost per watt, but is limited by relatively low power per unit area. Performance in all areas is expected to improve significantly.

## References

1. Catalano, A. et. al. " Solarex Annual Subcontractors Report", NREL/TP-411-4995 Aug. 1989

Sample #	1	2	3
Top i Layer Thickness	670 Å	840 Å	1000 Å
Short Circuit Current Under ELH	49.0 mA	54.4 mA	53.8 mA
Short Circuit Current Under LAPSS	44.1 mA	41.4 mA	37.4mA

Table 1. Short circuit currents for a series of samples under ELH and LAPSS illumination. The samples are identical tandem devices except for the thickness of the top i layer.

PARAMETERS @ 100mW/cm (@ 140mW/cm )	CURRENT PERFORMANCE LEVELS	EXPECTED PERFORMANCE LEVELS (2YRS)	POTENTIAL PERFORMANCE LEVELS
POWER/WEIGHT RATIO (W/KG)	550 W/KG (770 W/KG)	1760 W/KG (2460 W/KG)	2200 W/KG (3080 W/KG)
POWER/AREA RATIO (W/M <sup>2</sup> )	50 W/M <sup>2</sup> (70 W/M <sup>2</sup> )	80 W/M <sup>2</sup> (112 W/M <sup>2</sup> )	100W/M <sup>2</sup> (140W/M <sup>2</sup> )
COST/POWER \$/W	\$20/W (\$14.5/W)	\$10/W (\$7/W)	\$5/W (\$3.60/W)
PROCESS CONTROL	LOW YIELD	HIGH YIELD	HIGH YIELD

Table 2. Performance parameters for arrays showing current performance, performance expected in 1 to 2 years, and potential performance in the longer term. Parameters are based on 100 mW/cm. Data in parenthesis are for 140mW/cm to allow crude extension to AM0.

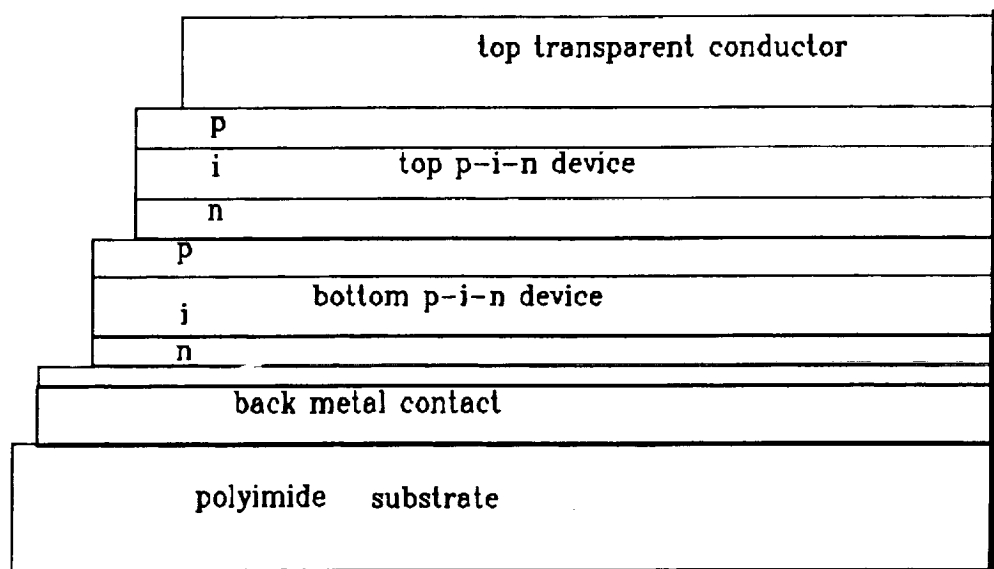


Figure 1. Diagram of the tandem a-Si device on polyimide substrate.

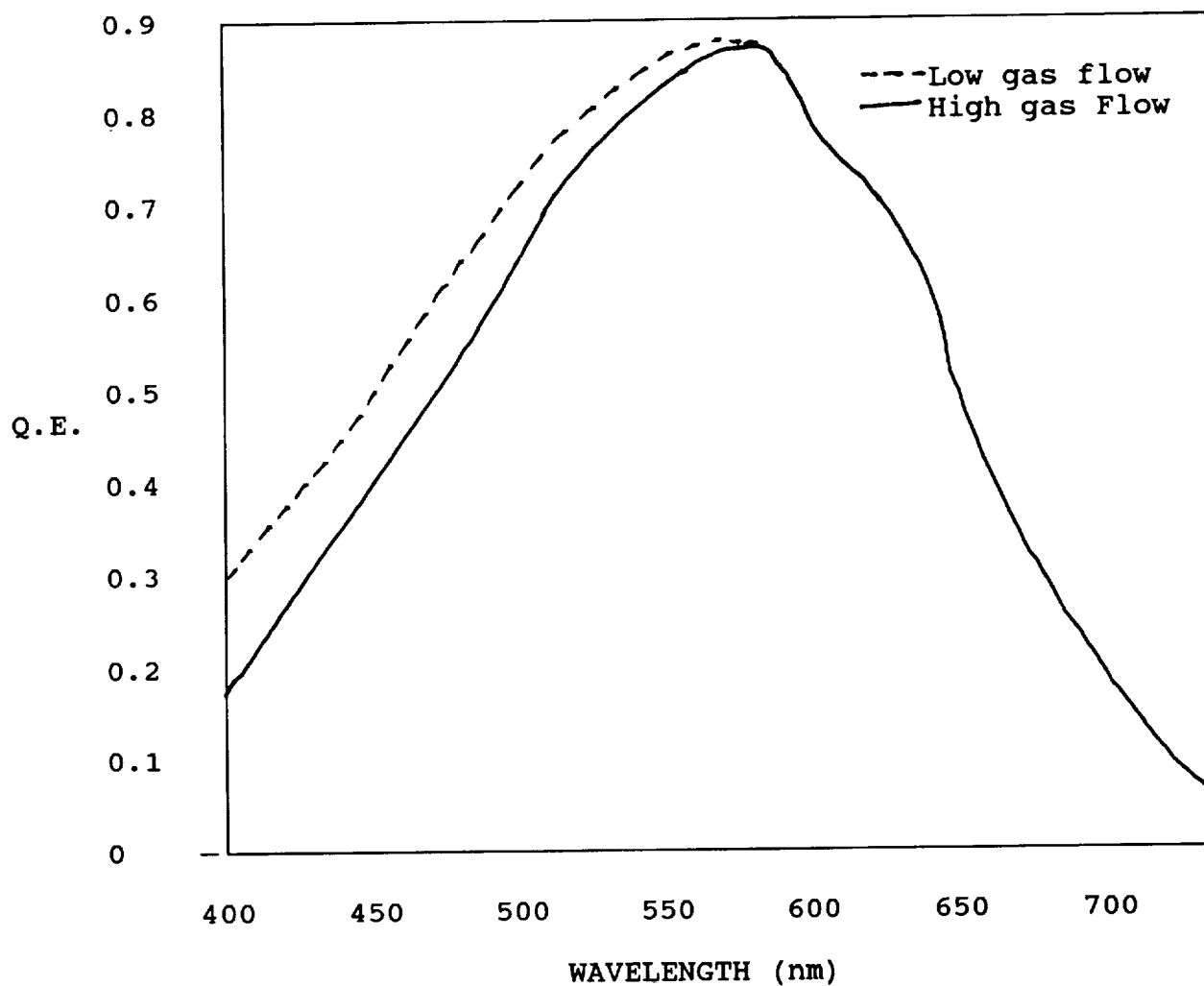


Figure 2. Quantum Efficiency data on two samples with p+ layers deposited under slightly different conditions. Gas ratios during p+ deposition were the same, but sample 2 had a higher total gas flow resulting in a higher deposition rate.

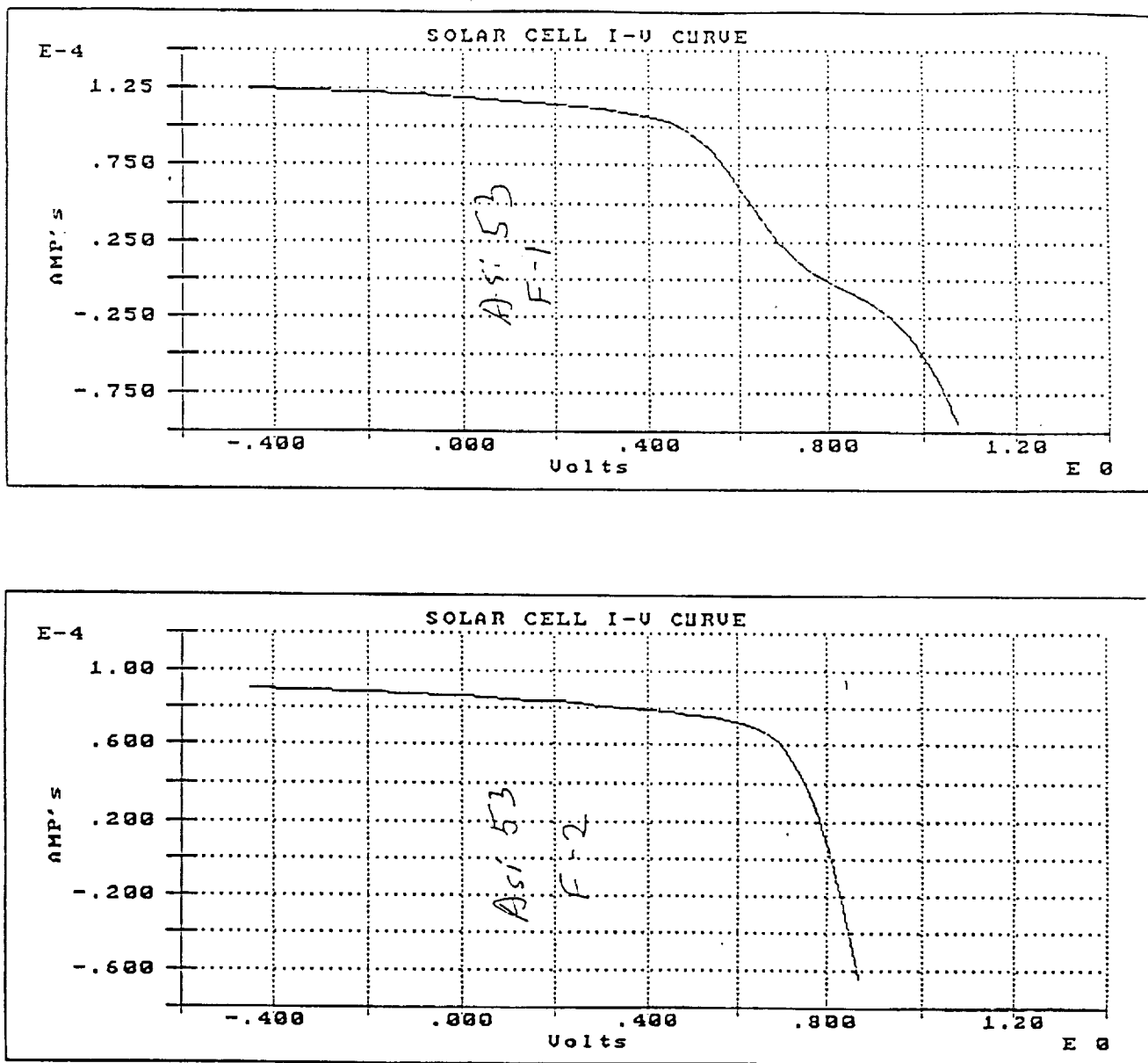


Figure 3. I-V curves for two n/p/i/n devices fabricated during the same run with 300 Watt (a) and 500 Watt (b) p<sup>+</sup> layers. The 300 Watt p<sup>+</sup> layer junction shows a reverse barrier at the tunnel junction while the 500 W p<sup>+</sup> layer junction shows excellent conduction.

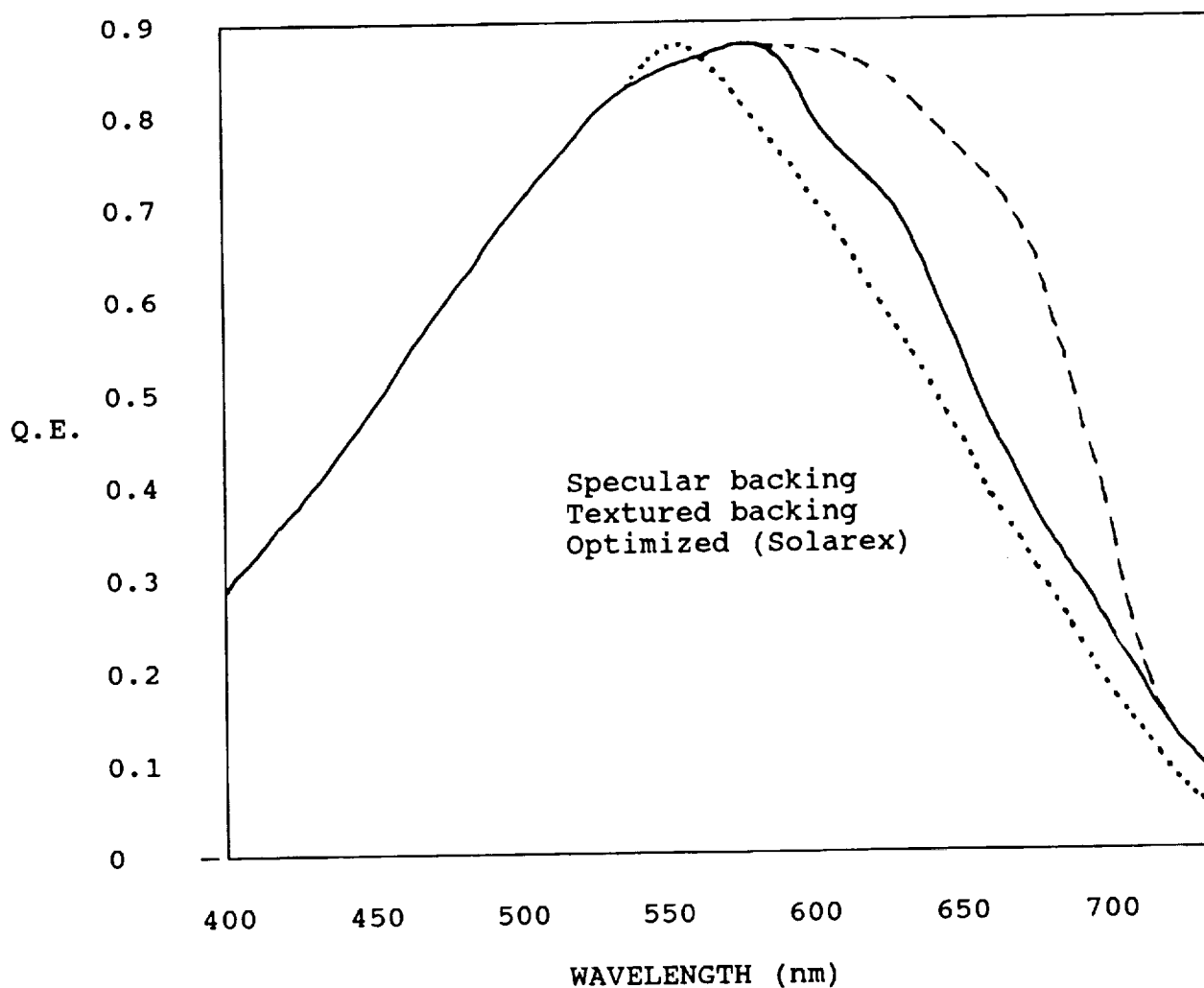


Figure 4. Quantum Efficiency data showing red response of devices with a specular back contact, our current textured back contact, and an optimized scattering and reflecting back contact from a Solarex superstrate device (ref 1).



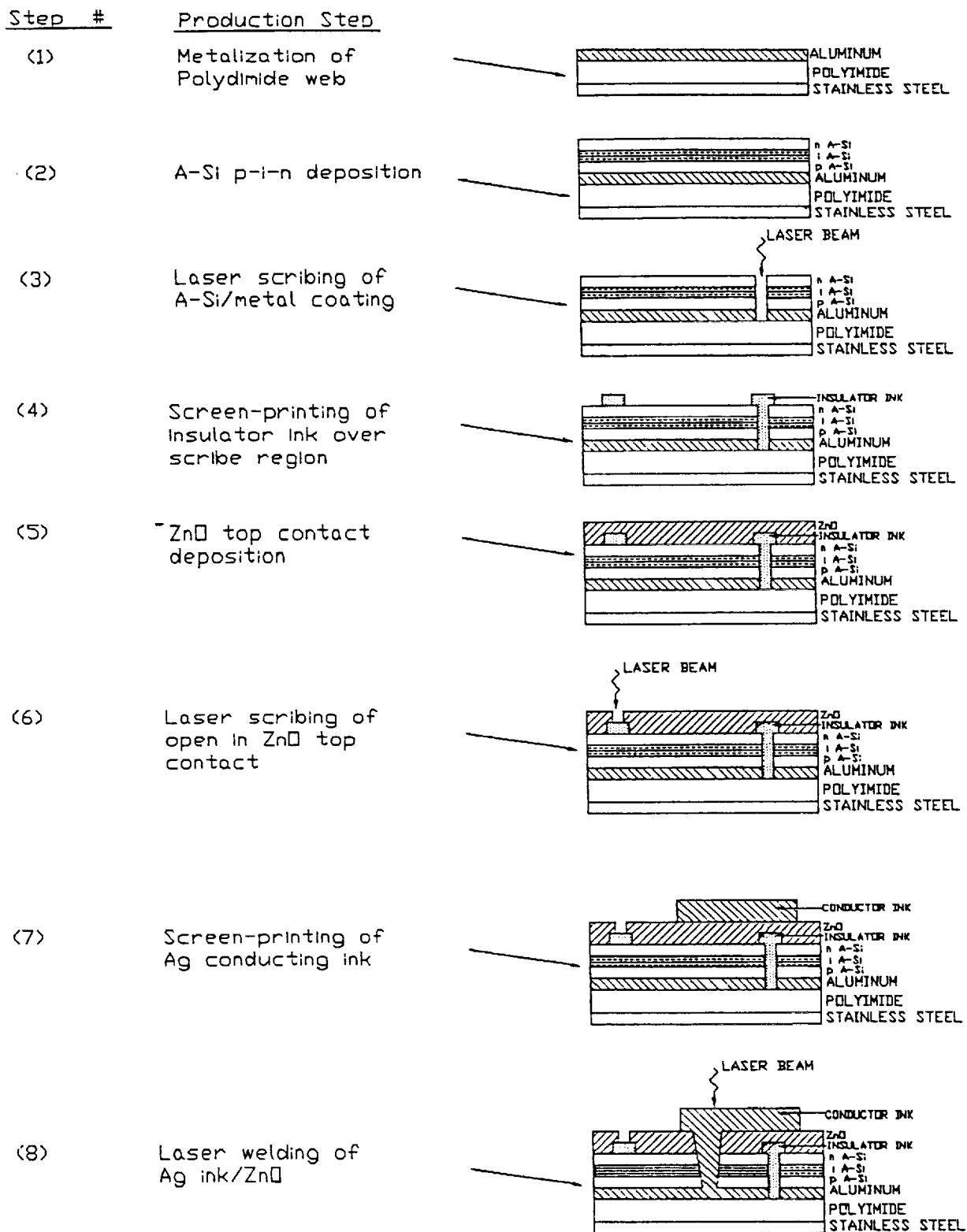
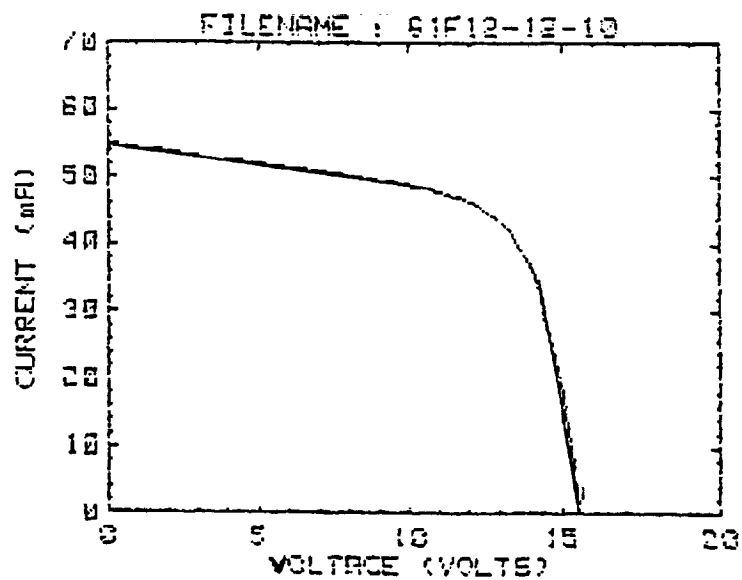


Figure 5. Structure of the monolithic interconnects used in the modules and the sequence of process steps needed to fabricate them.



Post  $V(oc)=15.607$  volts  
 $I(sc) = -.054959$  A  
 Fill Fctr = .660143  
 $V(maxpwr) = 12.818$  volts  
 $I(maxpwr) = -.044175$  A

Figure 6. I-V curve of a module demonstrating performance of devices coming from the current manufacturing level.